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LETTER TO THE EDITOR

Electron states at a solid C_{60}/Si(111) interface

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Abstract. Electron states at a solid C_{60}/Si(111) interface have been studied by the deep-level transient spectroscopy (DLTS) technique. An electron trap, $E_{it}(0.31)$, and three hole traps, $H_{it1}(0.27)$, $H_{it2}(0.36)$ and $H_{it3}(0.47)$, exist at the solid C_{60}/Si interface. H_{it1} and E_{it} are the dominant deep levels with densities of the order of magnitude 10^{11} cm^{-2}, and both of them probably originate from the dangling bonds on silicon(111) surfaces. The fact that the density of the interface states at the C_{60}/Si(111) interface is low indicates that C_{60} passivates the Si surface.

The discovery of a convenient method of preparing fullerenes in large quantities [1, 2] has stimulated a great many experimental studies on solid C_{60} films. It has been found that solid C_{60} films doped with alkaline metals can be superconducting [3] while undoped C_{60} films are insulating or semiconducting and have important electrical and optical properties [4–13]. Recently, studies have shown that there is a strong interaction between solid C_{60} films and Si substrates [11–18]. Scanning tunnelling microscopy (STM) and scanning tunnelling spectroscopy (STS) studies have confirmed that the C_{60} molecules form strong bonds with the Si substrate and this is associated with a significant charge transfer from Si substrate into C_{60} [16]. Studies on the electrical and optical properties of the solid C_{60}/Si contact have shown that both solid C_{60}/n-Si and C_{60}/p-Si are strong rectifying heterojunctions, and the rectification ratios are greater than 10^4 at ± 2 V [11–13] and the photovoltage may reach 0.4 V [17]. Studies on the structure of a C_{60} film on a silicon substrate reveal that the surface states of the Si substrate have a critical effect on the quality of the C_{60} film deposited on it [18]. It can be predicted that the quality of the solid C_{60}/Si interface has a remarkable effect on the characteristics of the heterojunction mentioned above; however, few reports have been presented on this subject.

The present work reports on the measurements for the interface states at the C_{60}/Si interface. Two main deep levels $H_{it1}(0.27)$ and $E_{it}(0.31)$ are observed at the C_{60}/Si interface and are considered to originate from the dangling bonds on the Si(111) surface. The dangling bond densities are greatly reduced by the interaction of C_{60} and the Si(111) surface.

Two kinds of sample were used in this article: (i) solid C_{60}/n-Si, with n-type single-crystalline silicon wafers (111) oriented and having a resistivity of 30 Ω cm; (ii) solid C_{60}/p-Si, with p-type single-crystalline silicon wafers (111) oriented and having a resistivity of 40 Ω cm. In order to obtain a good ohmic contact, gold films ($\simeq$500 nm) and aluminium films ($\simeq$1000 nm) were deposited on the back surfaces of n-Si and p-Si substrates, respectively, and they were annealed at 440 and 500 °C, respectively, in N_2 atmosphere for 30 minutes. The silicon wafers were dipped in a HF:H_2O = 1:20 solution to remove any

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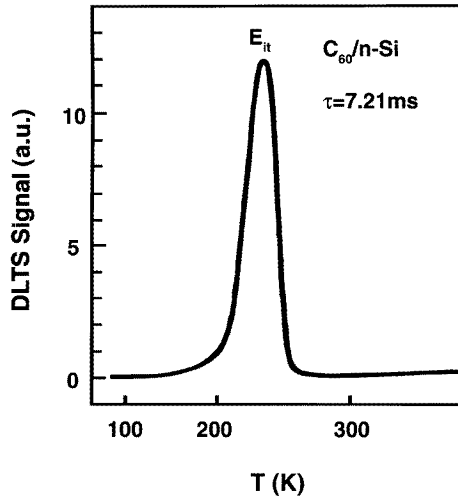

Figure 1. The DLTS spectrum of the solid C_{60}/n-Si heterojunction, rate window $\tau = 7.21$ ms, $V_R = -5$ V, $V_p = 5$ V and $t_p = 1$ ms.

oxide on their surfaces. The substrates were then cleaned by deionized water and dried with high-purity N_2 gas blowing, and conveyed immediately into an ultrahigh-vacuum (UHV) chamber for C_{60} deposition. C_{60} (99.9% purity) powders were prepared by the conventional AC arc method and purified by repeatedly performing liquid chromatography. The deposition of C_{60} film was performed in a BALZERS UMS-500 UHV system with a chamber pressure of 10^{-9} torr at a silicon substrate temperature of 200 °C. The deposition rate was ~1 nm min^{-1} and the C_{60} film thickness was monitored *in situ* by a quartz-crystal oscillator. The C_{60} films obtained were polycrystalline with a face-centred cubic structure, which was verified by low-energy electron diffraction pattern measurements. Titanium electrode dots of area 5.03×10^{-3} cm^2 were then evaporated onto the C_{60} films at 100 °C in the same UHV system. The final thicknesses of the C_{60} films were measured to be around 200 nm by use of a surface profiler (Sloan: Dektak 3030 ST).

The deep levels in the samples were measured by the deep-level transient spectroscopy (DLTS) technique. For the C_{60}/n-Si samples, the bias condition was as follows: reverse bias $V_R = 5$ V; pulse height $V_p = 5$ V, and pulse width $t_p = 1$ ms. A typical DLTS spectrum of solid C_{60}/n-Si with only one large peak at a temperature of around 263 K is shown in figure 1. The electron trap corresponding to this peak was denoted as E_{it}.

Figure 2 shows the relationship between the electron thermal emission rate of E_{it} traps at the C_{60}/n-Si interface and temperature (circles). The apparent electron activation energy and electron capture cross-section are determined to be 0.31 eV and 6.5×10^{-19} cm^2, respectively. The density of E_{it} is evaluated to be 1.1×10^{11} cm^{-2} by the high-frequency capacitance–voltage (CV) measurement and the DLTS peak height in figure 1.

Figure 3 shows the variation in the DLTS peaks of the electron trap E_{it} with the rate window at the sampling time ratio $t_1/t_2 = \frac{1}{2}$. It can be seen from this figure that the DLTS peak height of E_{it} increases by about a factor of two when the sample time t_2 is reduced from 50 to 0.5 ms. Fixing the sampling time ratio t_1/t_2, the increase in DLTS peak height with the rate window indicates that the traps corresponding to the peak probably exist at the interface i.e. $E_{it}(0.31)$ is likely to be an interface defect.

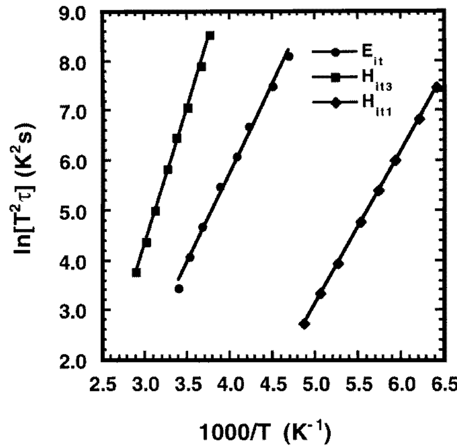

Figure 2. The relationships of the electron thermal emission rate of E_{it}, and the hole thermal emission rates of H_{it1} and H_{it3}, versus reciprocal temperature.

Two facts prove that $E_{it}(0.31)$ is an electron trap at the solid C_{60}/n-Si interface. One is that the DLTS measurement of a Ti/n-Si Schottky diode (a control sample) made on the same substrate as that of the C_{60}n-Si shows no observable deep level in the Si substrate. The other is that the C_{60} film of a solid C_{60}/n-Si heterojunction is an undoped and weak n-type semiconductor with a resistivity of $5 \times 10^6\ \Omega$ cm and the Fermi level is near the middle of the solid C_{60} energy gap. In such a semiconductor, only the electron trap near the mid-gap with a large electron capture cross-section can be detected by the DLTS technique under the bias conditions used for figure 1. If a defect such as E_{it}, with a level which is not sufficiently deep and a very small electron capture cross-section, were in the solid C_{60} it could not be measured under the measurement conditions for figure 1. Therefore, E_{it} is located in neither the n-Si nor the solid C_{60}, but at the C_{60}/n-Si interface.

A typical DLTS spectrum of solid C_{60}/p-Si samples under the bias condition of $V_R =$ 10 V, $V_p = -10$ V and $t_p = 1$ ms is shown in figure 4. The three hole traps corresponding to the three DLTS peaks in figure 4 are denoted by $H_{it1}(0.27)$, $H_{it2}(0.36)$ and $H_{it3}(0.47)$, respectively. In figure 2 the diamonds and squares show the relationships between hole thermal emission rates and temperature for $H_{it1}(0.27)$ and $H_{it3}(0.47)$, respectively, from which the apparent hole activation energy and the hole capture cross-section are determined, respectively, to be 0.27 eV and 1.2×10^{-16} cm^2 for H_{it1}, and 0.47 eV and 7.9×10^{-17} cm^2 for H_{it3}.

In order to determine the space position of the three hole traps, we performed a DLTS measurement on a Ti/p-Si junction (a control sample) fabricated on the same substrate as that of the C_{60}/p-Si sample. The results show that there is no observed deep level in the p-Si substrate. This indicates that the three hole traps do not belong to the p-substrate. For the same reasons as those for the electron trap E_{it} in C_{60}/n-Si, the three hole traps are not located in the solid C_{60} film either. Therefore, the three hole traps must be located at the interface of C_{60}/p-Si. The main parameters of the electron trap and the three hole traps are listed in table 1.

The origins of the traps E_{it}, H_{it1}, H_{it2} and H_{it3} at the solid C_{60}/Si interface can be analysed as follows. Since the Si(111) surface was not passivated intentionally before the C_{60} film was deposited, a large number of dangling bonds of silicon must exist there. Recent

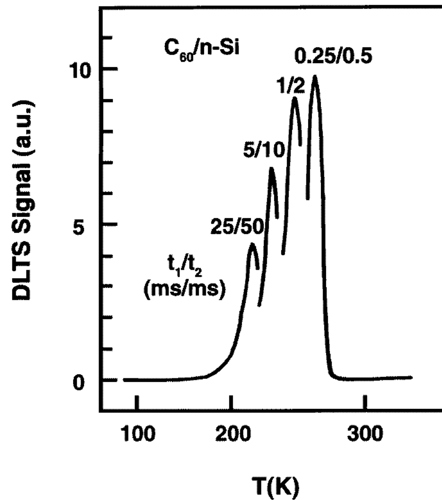

Figure 3. Variation in the DLTS peaks of the electron trap E_{it} with the rate window $t_1/t_2 = \frac{1}{2}$, $V_R = -5$ V, $V_p = 5$ V and $t_p = 1$ ms.

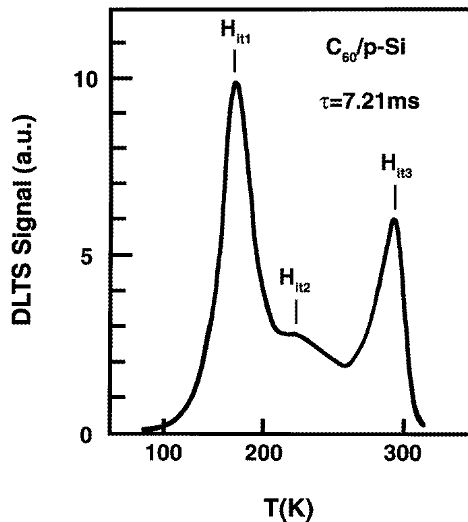

Figure 4. The DLTS spectrum of the solid C_{60}/p-Si heterojunction, $V_R = 10$ V, $V_p = -10$ V, $t_p = 1$ ms and $\tau = 7.21$ ms.

experiments indicate that these kinds of defect will strongly affect the deposition process of C_{60} on the Si surface and the quality of the C_{60} films deposited [18]. Some double bonds of C_{60} molecules may be broken to form C dangling bonds due to disturbance of the Si dangling bonds. Besides Si and C dangling bonds, a variety of impurities may also exist at the interface.

It can be seen from table 1 that the density difference between E_{it} and H_{it1} is within the error range of the DLTS measurement. So we could consider that they have almost identical densities. The energy levels of H_{it1} and E_{it} at 0 K are located at $E_v + 0.27$ eV

Table 1. The electrical parameters of E_{it}, H_{it1}, H_{it2} and H_{it3}.

Trap	Activation energy (eV)	Carrier capture cross-section (cm^2)	Density (cm^{-2})
E_{it}	0.31	6.5×10^{-19} (electron)	1.1×10^{11}
H_{it1}	0.27	1.2×10^{-16} (hole)	9.9×10^{10}
H_{it2}	0.36	—	6.8×10^{8}
H_{it3}	0.47	7.9×10^{-17} (hole)	5.3×10^{9}

and $E_v + 0.86$ eV, respectively, and the energy gap between them is 0.59 eV. Studies on electron states at the Si/SiO_2 interface [19–24] have confirmed that in the process of thermal oxidation without post-annealing, a dominant defect, the trivalent Si ($\bullet Si \equiv Si_3$), also called the P_b centre, exists at the interface. This defect is an amphoteric centre with a donor level located at $E_v + 0.26$ eV and an acceptor level at $E_v + 0.84$ eV [24]. Comparing our measurement with these results, H_{it1} and E_{it} are possibly the two energy levels of a silicon dangling bond.

The density of the interface states observed at the C_{60}/Si(111) interface is only in the order of magnitude of 10^{11} cm^{-2} while the defect density of the original silicon(111) surface should be in the order of 10^{15} cm^{-2}. The defect densities at the C_{60}/Si(111) interface are far smaller by comparison with that at the original silicon (111) surface. Possible reasons for sharply reducing the number of interface defects are various, for instance, the hydrogen adsorption on Si(111) surfaces caused by dipping the samples in the HF:H_2O = 1:20 solution was not removed completely in the ultrahigh-vacuum (UHV) system, and the oxygen in air moves through the solid C_{60} layer and reaches the C_{60}/Si interface. However, the fact that the interaction between the broken C double bonds of C_{60} and the silicon dangling bonds to form covalent bonds perhaps plays a leading role. This means that a solid C_{60} film can passivate the silicon surface.

In summary, we have observed two dominant deep levels, H_{it1} and E_{it}, at the solid C_{60}/Si interface. Most probably, they originate from silicon dangling bonds (P_b centres). The density of C_{60}/Si interface states is only 10^{11} cm^{-2}, indicating that solid a C_{60} film can passivate the silicon surface.

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